AMENDMENTS TO THE SPECIFICATION:

- *Please replace the paragraph extending from page 8 line 26 to page 9 line 3 with the following*:

  Whether a lookup table 60 or an algorithm is used, the resulting phase figure 62 reflects a weighted influence of each of the k data bits on phase (or phase error). The ~~weighing~~ weighting factors are merely multipliers applied to each data bit. For an algorithm, the multipliers will be obvious. For a lookup table 60, the different multipliers are inherent in developing the lookup table 60 and are thus reflected in the output from the table. The different multipliers are preferably related to chronological proximity of each data bit to the most delayed sample, wherein more recent data bits (nearer the center of the register) are weighed heavier than early or late data bits (nearer the edges of the register).

- *Please replace the two consecutive paragraphs from page 10 line 18 to page 11 line 12 with the following*:

  It is a feature of GMSK modulation that $d\theta/dt$ inverts on every Q bit. Since the register 58 operates on alternating I and Q bits, a combination alternate bit switch 64 and ~~compliment~~ complement block 68 are imposed as shown to correct the sign of the Q bits (which are inverted for GMSK as above). The phase figure 62 (for example, the nth bit which corresponds to the most recent data bit in the register 58 being an in phase bit) passes directly through the alternate bit switch block 64 without modification. The alternate bit switch block 64 then switches to receive the next succeeding phase figure (for example, the $n^{th}+1$ bit which corresponds to the most recent data bit in the register 58 being a quadrature bit) from the ~~compliment~~ complement block 68. The alternate bit switch block 64 receives only one input at an given instant, alternating between an input directly from the lookup table 60 and an input from the ~~compliment~~ complement block 68. Since the example n^{th} bit was an in phase bit, the next succeeding $n^{th}+1$ bit is necessarily a quadrature component. The quadrature $n^{th}+1$ reconstructed phase passes through the

2

compliment block 68, which takes the ~~compliment~~ complement of the phase (one quarter cycle minus the phase) for the quadrature bits. The alternating bit switch block 64 thus alternates its output between in phase and quadrature bits. This allows the same lookup table 60 to be used at the in-phase and quadrature bit times.

The adder 70 takes as inputs the phase estimate ~~62~~ from the lookup table 60 (the phase estimate being either the phase figure 62 for the I bits or the ~~compliment~~ complement of the phase figure 62 for the Q bits), and a phase offset from the phase loop filter 80. Adding these two inputs at the adder 70 yields a reconstructed phase correction.

- *Please replace the two consecutive paragraphs from page 12 line 4 to page 13 line 1 with the following:*

As noted above, phase and timing error in a CPM waveform are related. The present invention provides that timing correction may be made with the same lookup table 60 that was used for phase correction. Along with the phase figure 62, the lookup table 60 also outputs a symbol tracking signal 66. Preferably, the symbol tracking signal 66 is the time derivative of the phase, $d\phi/dt$. In this manner, a single, relatively abbreviated lookup table 60 may be used to generate both outputs, phase figure 62 and symbol tracking signal 66. Where the symbol tracking signal 66 is the time derivative of the phase $d\phi/dt$, a feature of continuous phase modulation (CPM) is that every time derivative of phase $d\phi/dt$ that corresponds to a quadrature bit has an inverted sign (+ or -). In phase error correction, this was compensated by taking the ~~compliment~~ complement of the Q related phase figure 62. In timing error correction, this is compensated by passing every time derivative related to a Q bit through an alternate bit inverter 72. In short, every derivative corresponding to an I bit passes unchanged through the alternate bit inverter 72, and every derivative corresponding to a Q bit passes through the alternate bit inverter 72 with only

its sign (+ or -) changed. The output of the alternate bit inverter 72 is a (sign corrected) ~~weighing~~ weighting factor that is dependent upon the bit pattern stored in the register 58 at the time the relevant bit k first entered the register 58. This ~~weighing~~ weighting factor (the output of the alternate bit inverter 72) is input into a multiplier 74, which is part of the timing loop.

The timing loop comprises the timing adjust block 50, the delay circuit 76, the loop phase shifter 78, the multiplier 74, and a timing loop filter 82. Along with the output of the alternate bit inverter 72 as detailed above, one other input to the multiplier 74 is the output of the loop phase shifter 78, also detailed above. The output of the loop phase shifter 78 is a delayed version of the received signal that is phase compensated. Since the output of the alternate bit inverter 72 is just a ~~weighing~~ weighting factor, the multiplier applies that ~~weighing~~ weighting factor to the output of the loop phase shifter 78 to result in a timing offset signal. The timing offset signal that is output from the multiplier 74 is then passed through a timing loop filter 82, which filters out undesirable high frequency components, and input into the timing adjust block 50. There, the filtered timing offset signal is used to adjust the timing of the received CPM signal.

- *Please replace the title at page 19 lines 1-2 (above the abstract) with the following:*

PHASE CORRECTION FOR A PHASE MODULATED ~~WAVEFORM USING~~ ~~MULTIPLE DATA BITS~~ SIGNAL WITH MUTUALLY INTERFERING SYMBOLS